WHAT IS CLAIMED IS:

1. A semiconductor device, comprising:

first and second semiconductor substrates having respective opposite surfaces disposed in opposition to each other;

a first semiconductor element formed in said opposite surface of said first semiconductor substrate and comprised of a first semiconductor circuit and a first electrode;

a second semiconductor element formed in said opposite surface of said second semiconductor substrate and comprised of a second semiconductor circuit and a second electrode;

a first wiring conductor layer formed of an electrically conductive material and interposed between said first and second electrodes; and

a through electrode extending through said first semiconductor substrate and connected to said first and second electrodes through the medium of said first wiring conductor layer,

wherein said second semiconductor substrate is disposed above said first semiconductor substrate and disposed on a lateral side of said through electrode, being distanced therefrom;

wherein lateral surface of said through electrode projecting from said first semiconductor substrate and lateral surface of said second semiconductor element are coated with an insulation material layer;

wherein said through electrode has one end portion exposed from a back surface of said first semiconductor substrate to serve as a first external terminal; and

wherein said through electrode has the other end portion positioned at a same height as a back surface of said second semiconductor substrate and exposed from said insulation material layer to serve as a second external terminal.

2. The semiconductor device according to claim 1,

wherein said semiconductor device further includes a first additional external terminal exposed from a back surface of said first semiconductor substrate in a region in which said second semiconductor substrate is mounted.

3. The semiconductor device according to claim 1,

wherein the back surface of said second semiconductor substrate is coated with an insulation material.

4. The semiconductor device according to claim 3,

wherein said semiconductor device includes a second wiring conductor layer of an electrically conductive material deposited on a surface of the insulation material of said first and second semiconductor substrates and an exposed surface of said second external terminal, and

wherein said second wiring conductor layer is connected to said through electrode at a portion thereof which is exposed as said second external terminal.

5. The semiconductor device according to claim 1,

wherein an element interconnecting protrusion electrode is provided between said first electrode and said second electrode, and

wherein said first semiconductor element and said second semiconductor element are interconnected through the medium of said element interconnecting protrusion electrode.

6. The semiconductor device according to claim 1,

wherein a device connecting protrusion electrode projecting from the exposed surface of said through electrode is provided in association with at least one of said first external terminal and said second external terminal, and

wherein said device interconnecting protrusion electrode is employed as an external terminal.

7. The semiconductor device according to claim 1,

wherein an SOI (silicon oxide insulation) substrate is employed for forming said first semiconductor substrate, and

wherein an SOI insulation film is exposed as the back surface of said first semiconductor substrate.

8. The semiconductor device according to claim 7,

wherein a third wiring conductor layer is deposited on said SOI insulation film of said first semiconductor substrate, said third wiring conductor layer being connected to said first external terminal.

9. The semiconductor device according to claim 1,

wherein an SOI (silicon oxide insulation) substrate is employed as said

second semiconductor substrate, and

wherein said SOI substrate includes an exposed SOI insulation film formed in the back surface of said second semiconductor substrate.

10. The semiconductor device according to claim 1,

wherein a plurality of the semiconductor devices set forth in claim 1 is interconnected through the medium of said first external terminal and/or said second external terminal.

11. The semiconductor device according to claim 10,

wherein said semiconductor device further comprises

a third semiconductor substrate mounted on said second semiconductor substrate; and

a third semiconductor element formed in said third semiconductor substrate and comprised of a third semiconductor circuit and a third electrode,

wherein said third electrode is connected to said second external terminal, and

wherein lateral surface of said third semiconductor element and a surface of said third semiconductor substrate in which said third semiconductor circuit is formed are coated with an insulating material.

12. The semiconductor device according to claim 1,

wherein said through electrodes and said first semiconductor circuits are formed in pairs, respectively, in said first semiconductor substrate,

wherein said second semiconductor elements are disposed with said second electrodes being connected to the first electrodes of said plurality of first semiconductor circuit, respectively; and

wherein the surfaces of said first and second semiconductor substrate in which said first and second semiconductor circuits are formed, respectively, lateral surfaces of said second semiconductor substrates, and lateral surfaces of said through electrodes, respectively, are coated with an insulation material to thereby implement an integral planar array structure on a single board constituted by said first semiconductor substrate.

13. The semiconductor device according to claim 12,

wherein a plurality of semiconductor elements are stacked in at least one of said semiconductor devices connected to the first electrodes of said plurality

of first semiconductor circuits.

14. The semiconductor device according to claim 1,

wherein thickness of said first semiconductor substrate does not exceed 20 μm.

15. A method of manufacturing a semiconductor device, comprising:

a circuit forming step of forming a first semiconductor circuit including a connecting terminal portion on a first semiconductor substrate;

a hole forming step of forming a first hole of a predetermined depth reaching a semiconductor substrate matrix of said first semiconductor substrate at a position located outside of a region in which a second semiconductor element including a second semiconductor circuit and a second electrode formed previously in a second semiconductor substrate is to be disposed;

an insulation film deposition step of depositing a insulation film on a lateral wall and a bottom of said first hole and a surface of said first semiconductor substrate in which said first semiconductor circuit is formed;

an insulation film eliminating step of eliminating said insulation film formed on the bottom of said hole and said connecting terminal portion;

a wiring conductor connecting step of forming a wiring conductor layer of an electrically conductive material such that one end portion of said wiring conductor layer is connected to the semiconductor substrate matrix forming the bottom of said hole with other end portion thereof serving as a first electrode;

a resist pattern forming step of applying a resist on the side of said semiconductor substrate in which said first semiconductor circuit is formed to thereby form a resist pattern of a predetermined thickness, said resist pattern having an opening for forming said first hole;

an electrode forming step of forming a through electrode on said electrically conductive material through said opening formed in said resist pattern by electroplating with said first semiconductor substrate matrix being used as a cathode;

a resist removing step of removing said resist;

an element interconnecting step of connecting a first semiconductor element including said first semiconductor circuit and said first electrode formed in said first semiconductor substrate with said second semiconductor element through the medium of said first electrode and said second electrode;

a through electrode insulation coating step of coating said second semiconductor substrate and said through electrode with an insulation material on

the surface of said first semiconductor substrate in which said first semiconductor circuit is formed;

a surface grinding step of grinding the insulation material coated in said through electrode insulation coating step from a side of said first semiconductor substrate on which said second semiconductor substrate is mounted until said through electrode is exposed; and

a back surface grinding step of grinding a back surface of said first semiconductor substrate by a predetermined thickness.

16. The semiconductor device manufacturing method according to claim 15, further comprising:

a protruding electrode forming step of forming a protruding electrode on a top portion of said through electrode exposed on the side f said second semiconductor substrate through an electroplating process by using said first semiconductor substrate as a cathode, after said surface grinding step has been carried out.

17. The semiconductor device manufacturing method according to claim 15, further comprising:

a back surface etching step of eliminating by etching said semiconductor substrate matrix exposed on the back surface of said first semiconductor substrate until said through electrode protrudes from said first semiconductor substrate in succession to said back surface etching step.

18. The semiconductor device manufacturing method according to claim 15,

wherein in said hole forming step, a second hole is formed at a position distanced from said first hole by a predetermined distance with a predetermined depth reaching said semiconductor substrate matrix,

wherein in said insulation film depositing step, an insulation film is deposited on a lateral surface and a bottom of said second hole,

wherein in said insulation film eliminating step, said insulation film formed on the bottom of said second hole is removed,

wherein in said wiring conductor connecting step, a wiring conductor is formed with one end portion being connected to said connecting terminal,

wherein in said resist pattern forming step, a resist pattern of a predetermined thickness is formed in which an opening is formed at a location where

said second hole is to be formed, and

wherein in said electrode forming step, an electrically conductive material is buried into said second hole.

19. The semiconductor device manufacturing method according to claim 15,

wherein in said resist pattern forming step, the resist pattern is formed at a height higher than the back surface of said second semiconductor substrate which is located oppositely to the surface in which said second semiconductor circuit forming surface is formed,

wherein in said electrode forming step, said through electrode is formed at a height higher than the back surface of said second semiconductor substrate which is located oppositely to the surface in which said second semiconductor circuit is formed, and

wherein in said surface grinding step, only said through electrode is exposed.

20. The semiconductor device manufacturing method according to claim 15,

further comprising a surface conductor portion forming step in which the surface ground by said surface grinding step is coated with an insulation film pattern capable of accommodating a position of a top portion of said through electrode, to thereby form an electrically conductive portion which is connected to said top portion and which has a thickness not lower than a height of surface of said insulation film pattern through on electroplating by making use of said semiconductor substrate matrix of said first semiconductor substrate as cathode.